8256
MULTIFUNCTION UNIVERSAL ASYNCHRONOUS RECEIVER-TRANSMITTER (MUART)

- **Programmable Serial Asynchronous Communications Interface for 5-, 6-, 7-, or 8-Bit Characters, 1, 1½, or 2 Stop Bits, and Parity Generation**
- **Two 8-Bit Programmable Parallel I/O Ports; Port 1 Can Be Programmed for Port 2 Handshake Controls and Event Counter Inputs**
- **On-Board Baud Rate Generator Programmable for 13 Common Baud Rates up to 19.2K Bits/second, or an External Baud Clock Maximum of 1M Bit/second**
- **Eight-Level Priority Interrupt Controller Programmable for 8085 or iAPX 86, iAPX 88 Systems and for Fully Nested Interrupt Capability**
- **Five 8-Bit Programmable Timer/ Counters; Four Can Be Cascaded to Two 16-Bit Timer/Counters**
- **Programmable System Clock to 1×, 2×, 3×, or 5×1.024 MHz**

The Intel® 8256 Multifunction Universal Asynchronous Receiver-Transmitter (MUART) combines five commonly used functions into a single 40-pin device. It is designed to interface to the 8048, 8085A, iAPX 86, and iAPX 88 to perform serial communications, parallel I/O, timing, event counting, and priority interrupt functions. All of these functions are fully programmable through nine internal registers. In addition, the five timer/counters and two parallel I/O ports can be accessed directly by the microprocessor.

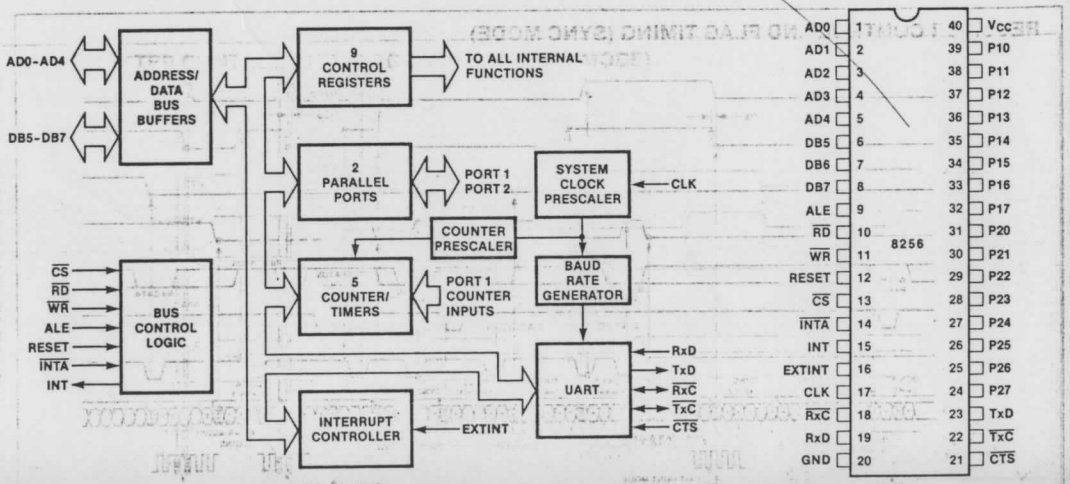

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
AD0-AD4 DB5-DB7	1-5 6-8	I/O	**Address/Data:** Three-State Address/Data lines which interface with the CPU lower 8-bit address/data bus. The 5-bit address is latched on the falling edge of ALE. In 8048 and 8085 mode, AD0-AD3 are used to select the proper register, while AD1-AD4 are used in 8086 and 8088 mode. The 8-bit bidirectional data bus is either written into or read from the chip depending on the latched $\overline{CS}$ and $\overline{RD}$ or $\overline{WR}$.
ALE	9	I	**Address Latch Enable:** Latches the 5 address lines on AD0-AD4 and $\overline{CS}$ on the falling edge.
$\overline{RD}$	10	I	**Read Control:** When this signal is low, the previously selected register is enabled onto the data bus.
$\overline{WR}$	11	I	**Write Control:** When this signal is low, the value on the data bus is placed into the previously selected register.
RESET	12	I	Pulse provided by the CPU to initialize the system. The MUART remains "idle" until it is reprogrammed by the CPU.
$\overline{CS}$	13	I	**Chip Select:** A low on this signal enables the MUART. It is latched with the address on the falling edge of ALE, and $\overline{RD}$ and $\overline{WR}$ have no effect unless $\overline{CS}$ was latched low during the ALE cycle.
$\overline{INTA}$	14	I	**Interrupt Acknowledge:** If the MUART has been enabled to respond to interrupts, it puts an RST on the bus for the 8085 or a vector for the 8086. The bit in the interrupt register is reset when the interrupt is placed onto the bus.
INT	15	O	**Interrupt:** A high signals the CPU that the MUART needs service.
EXTINT	16	I	**External Interrupt:** A high on this pin signals that an external device requests service. EXTINT must be held high until $\overline{INTA}$ or read interrupt occurs.
CLK	17	I	**System Clock:** This input provides an accurate timing source for the MUART. It must be 1×, 2×, 3×, or 5× 1.024 MHz and is used by the baud rate generator and real time clocks.
$\overline{RxC}$	18	I/O	**Receive Clock:** If baud rate 0 is selected, this input clocks bits into RxD on the rising edge. If a baud rate from 1-$0F_{16}$ is selected, this output will provide a rising edge at the center of each received data bit. This output remains high during start, stop, and parity bits.
RxD	19	I	**Receive Data:** Serial data input from the modem or terminal to the MUART.
GND	20	PS	**Ground:** Power supply and logic ground reference.

Symbol	Pin No.	Type	N
V_{CC}	40	PS	**Power:** +5V
P17-P10	32-39	I/O	**Parallel I/O** grammed a perform ge for the CPU addition to programme functions counter in munication
P27-P20	24-31	I/O	**Parallel I/O** of this port output. Also bidirectiona lines in Por
TxD	23	O	**Transmit D** serial data from the MU
$\overline{TxC}$	22	I/O	**Transmit C** this input c mitter on th of 1 or 2 is the user to which is us mitter. If th internal tra 1½ stop characters ted, the inte be reset at the clock spike instea low transiti each bit an the center
$\overline{CTS}$	21	I	**Clear to Se** serial trans character i be sent. A causes the previously transmitter when the b transmissio the first sto baud rate f must be low will be igno